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Adaptive Dual-MAF Weighted SRF-PLL with Online Self-Tuning PI Control for DSTATCOM Power Quality Enhancement

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Abstract
This paper proposes an Adaptive Dual-Moving-Average-Filter Weighted Synchronous Reference Frame Phase-Locked Loop (Adaptive Dual-MAF Weighted SRF-PLL) with online self-tuning proportional–integral (PI) control for power-quality enhancement using a three-phase Distribution Static Compensator (DSTATCOM). The proposed synchronization scheme processes the quadrature-axis phase-error signal through parallel short- and long-window moving-average filters to combine fast tracking with improved disturbance attenuation. Unlike fixed-weight structures, the relative contribution of the two MAF outputs is adjusted online using a normalized-gradient adaptation law with projection and complementary-weight constraints. A bounded disturbance index is additionally employed to regulate the adaptation rate and PLL dynamics according to the instantaneous synchronization condition. Online adaptive self-tuning PI regulators are incorporated into the DC-link and PCC-voltage control loops to accommodate variations in operating conditions while maintaining bounded controller gains. The complete control scheme is implemented on a SPARTAN-6 FPGA-based DSTATCOM prototype and experimentally evaluated under nonlinear, unbalanced, and dynamic load conditions. The measured RMS source currents are 6.98A, 6.93A, and 7.00A for phases a, b, and c, respectively, with corresponding current THDs of 3.52%, 3.49%, and 3.91%. The experimental results further demonstrate balanced source currents during load asymmetry, effective reactive-current compensation, and stable regulation of the 220-V DC link during load transitions. These results confirm the suitability of the proposed adaptive synchronization and control structure for real-time DSTATCOM-based power-quality compensation.

Keywords: Adaptive Dual-MAF, DSTATCOM, SRF-PLL, adaptive weighting, self-tuning PI control, power quality.

1. Introduction

The increasing penetration of nonlinear loads, power-electronic converters, adjustable-speed drives, and distributed energy resources has intensified power-quality concerns in modern distribution networks. Such loads may introduce harmonic currents, reactive-power demand, load imbalance, and deterioration of the source-current waveform. These effects increase network losses, reduce equipment utilization, and may adversely influence sensitive loads. Consequently, effective compensation of current harmonics and reactive power remains an important requirement in distribution systems [1], [2]. A distribution static compensator (DSTATCOM), implemented using a voltage-source converter (VSC), provides a flexible shunt-compensation solution because it can generate compensating currents according to the instantaneous load and grid conditions.

The performance of a DSTATCOM is strongly influenced by its control and synchronization algorithms. In synchronous-reference-frame-based compensation, reliable estimation of the grid phase angle is particularly important because the estimated angle directly influences the transformation of measured quantities and the subsequent generation of reference currents. Arya et al. used MAF-PLL, DSOGI-PLL, and adaptive-filter-with-frequency-estimation-loop PLL (AFFEL-PLL) synchronization methods to investigate PLL-based DSTATCOM control under nonlinear and unbalanced load conditions [3]. A later comparative analysis evaluated various PLL architectures for DSTATCOM operation under unbalanced and distorted grid conditions to examine how fundamental-component extraction affects compensation performance [4]. Later research on DSTATCOM focused on developing new compensation and adaptive control methods [5], [6] and on developing PLL architectures that allow better operation under non-ideal grid conditions [7], [8].

Research in recent years shows that improved synchronization can lead to better DSTATCOM compensation performance. Özer et al. presented a fast hybrid PLL for a DSTATCOM-supported wind energy system and evaluated it under nonlinear and unbalanced loads, open-circuit faults, and measurement offsets [9]. Their evaluation showed the importance of both disturbance rejection and rapid phase and frequency estimation. An MAF-based dq-control method has also been developed for DSTATCOM-supported systems. In that development, moving average filters were used to reduce the harmonic content during reference-current determination. This made voltage and frequency regulation possible under nonlinear and unbalanced load conditions [10]. These studies clearly show that the synchronization block is not merely an auxiliary module; it can be very significant in determining the quality of the compensated source currents.

Several types of grid-synchronization techniques are available today. Among them, the synchronous reference frame PLL (SRF-PLL) is widely used because of its simplicity, ease of implementation, and compatibility with dq-frame converter control. Nonetheless, distorted and unbalanced grid voltages generate oscillations in the synchronous reference frame that can negatively affect phase and frequency estimation. Additionally, the nonlinear phase-detection characteristics of conventional SRF-PLLs require attention when there are significant differences between actual operating conditions and nominal operating conditions [11]. Therefore, several authors have implemented different filtering schemes within PLL structures to improve their disturbance-rejection capabilities while limiting the computational burden. Moving Average Filters (MAFs) provide a good example in this regard. They offer a computationally efficient filtering solution that can effectively suppress periodic disturbances. Liu et al. described an enhanced version of the MAF-based PLL suitable for grid-connected applications [12]. Martinz et al. studied the dynamic response properties of MAF-based synchronization techniques [13]. Li et al. developed an αβ-frame MAF scheme to improve PLL dynamics [14]. Studies such as these show an essential design tradeoff: increasing the averaging-window length generally enhances the filtering capability against disturbances; however, it also increases the filtering delay. On the other hand, decreasing the averaging-window length shortens the transient response of PLLs; however, it can reduce their disturbance-rejection capability. This tradeoff between filtering capability and dynamic response thus forms one of the most relevant considerations in designing MAF-based PLLs.

To mitigate this tradeoff, researchers have pursued adaptive solutions. For example, Luo and Wei developed a frequency-adaptive improved MAF-based quasi-type-1 PLL for adverse grid conditions, providing solutions to some of the drawbacks of conventional MAF-QT1 PLL implementations related to transient response and frequency-dependent behavior during grid-frequency variations [15], [16]. Similarly, Taheri et al. introduced a variable-window-size MAF for PLL synchronization [17], [18], in which the averaging window is dynamically adjusted according to the predominant oscillation component. As a result, they achieved improved dynamic-response performance while preserving adequate disturbance-rejection capability. Smadi et al. [19] proposed an enhanced third-order PLL combining MAF-based filtering with arbitrarily delayed signal cancellation (ADSC) to improve synchronization performance under distorted grid conditions. Although the method achieves effective suppression of harmonic components and DC-offset disturbances and uses a reduced filtering window for faster transient response, its filtering structure does not incorporate adaptive weighting between multiple parallel MAF channels.

In contrast, Kathiresan et al. [20] designed an adaptive feed-forward PLL that allows stable grid synchronization under wide grid-frequency deviations. A frequency-adaptive FIR filter adjusts its gain according to the estimated grid frequency so that accurate phase and frequency tracking can be maintained under harmonic distortion, voltage imbalance, and frequency deviations. However, the method does not employ adaptive weighting between parallel MAF channels. Recently, Kumar et al. developed an in-loop comb-filter-based PLL architecture [21] that selectively attenuates the negative-sequence component and dominant lower-order harmonic components and employs PID regulation to enhance the dynamic response. Their study further emphasizes the need to develop robust synchronization algorithms that can eliminate disturbing components without introducing excessive delay or high computational complexity.

Research gap

A research gap exists in relation to the synchronization of DSTATCOMs. In spite of recent advancements regarding the synchronization of DSTATCOMs, conventional phase-locked loop (PLL)-based moving average filter (MAF) synchronization systems have inherent limitations. A significant limitation of many existing PLL-based MAF synchronization schemes is that they rely on a single filtering path or a predefined filtering characteristic, while adaptive techniques typically adjust the averaging-window length, frequency-dependent parameters, prefiltering stage, or loop dynamics. As a result, a single fixed-window MAF cannot simultaneously provide the fast transient response associated with a short averaging window and the strong disturbance attenuation associated with a long averaging window. Similarly, a fixed or predefined combination of two

filtering paths results in a predetermined compromise and does not permit dynamic redistribution of the contribution of each path according to changing operating conditions.

Proposed work and original contributions

To address this issue, an Adaptive Dual-MAF Weighted SRF-PLL is proposed for DSTATCOM power-quality enhancement. The quadrature-axis synchronization error is processed simultaneously through short- and long-window MAF paths. Rather than combining these outputs using predetermined coefficients, their contributions are adjusted online through a normalized-gradient adaptive weighting mechanism. The weight update is subjected to projection and complementary constraints to maintain bounded coefficients satisfying $W_1 + W_2 = 1$. Thus, the proposed structure preserves two complementary filtering characteristics and dynamically regulates their participation in forming the PLL error. The resulting synchronization signal is subsequently used for phase estimation and DSTATCOM reference-current generation.

The main contributions of this work are summarized as follows:

1. A parallel Dual-MAF SRF-PLL structure is developed to retain the fast dynamic characteristic of a short-window MAF and the stronger filtering characteristic of a long-window MAF within a unified synchronization framework.
2. A normalized-gradient adaptive weighting mechanism is introduced to regulate the contribution of the two MAF outputs online, together with projection and complementary-weight constraints for bounded operation.
3. The adaptive synchronization mechanism is integrated into the DSTATCOM control scheme for harmonic-current mitigation, reactive-power compensation, source-current balancing, and power-factor improvement.
4. The proposed controller is evaluated under steady-state and disturbed operating conditions and compared with the preceding PLL-based DSTATCOM schemes using synchronization response and power-quality indices.

The remainder of this paper presents the DSTATCOM system configuration, develops the proposed Adaptive Dual-MAF Weighted SRF-PLL and associated reference-current control, and subsequently evaluates its performance through comparative simulation and experimental investigations.

2. System Configuration

Fig. 1 shows the configuration of a three-phase, three-wire distribution system equipped with a voltage-source-converter (VSC)-based DSTATCOM at the point of common coupling (PCC). The system consists of a three-phase AC source, source impedance, nonlinear load, and shunt-connected DSTATCOM. The DSTATCOM employs a three-leg VSC supported by a DC-link capacitor C_{dc} and is coupled to the PCC through interfacing inductors L_f.

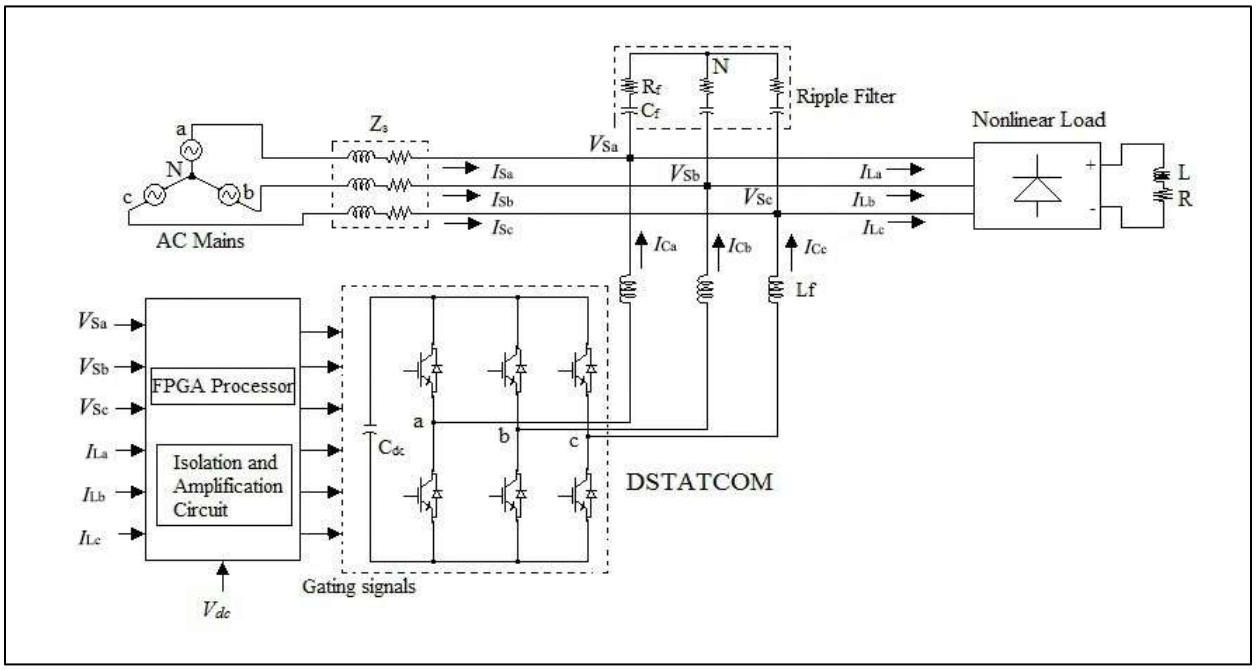


Fig. 1. Three-phase VSC-based DSTATCOM topology

These inductors limit the switching-current ripple and facilitate controlled compensating-current injection. A $R_f - C_f$ ripple filter connected at the PCC suppresses high-frequency switching components generated by the VSC [22]-[24]. The compensating currents (i_{Ca}, i_{Cb}, i_{Cc}) are injected to compensate for the harmonic and

reactive components drawn by the nonlinear load. The proposed Adaptive Dual-MAF Weighted SRF-PLL accurately tracks the grid phase angle required for reference-current generation. Meanwhile, the DC-link voltage is regulated at its reference value to ensure stable and continuous operation of the DSTATCOM.

3. Adaptive Dual-MAF Weighted SRF-PLL control with Online Adaptive Self-Tuning PI for DSTATCOM

Accurate estimation of the grid phase angle is essential for synchronous-reference-frame-based control of a DSTATCOM. The proposed Adaptive Dual-MAF Weighted SRF-PLL processes the measured three-phase PCC voltages through synchronous-reference-frame transformation, parallel moving-average filtering, constrained adaptive weighting, and adaptive PLL gain regulation to estimate the instantaneous grid phase angle as shown in Fig.2. The adaptive structure is designed to combine the fast response of a short-window MAF with the stronger disturbance attenuation of a long-window MAF while modifying the PLL dynamics according to the instantaneous synchronization condition.

A. Synchronous Reference-Frame Transformation

The measured three-phase PCC voltages $V_{sa}(t)$, $V_{sb}(t)$, and $V_{sc}(t)$ are transformed from the stationary abc frame into the synchronous dq reference frame using the estimated phase angle $\hat{\theta}(t)$ as expressed in (1).

$$\begin{bmatrix} V_d(t) \\ V_q(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\hat{\theta} & \cos\left(\hat{\theta} - \frac{2\pi}{3}\right) & \cos\left(\hat{\theta} + \frac{2\pi}{3}\right) \\ -\sin\hat{\theta} & -\sin\left(\hat{\theta} - \frac{2\pi}{3}\right) & -\sin\left(\hat{\theta} + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} V_{sa}(t) \\ V_{sb}(t) \\ V_{sc}(t) \end{bmatrix} \quad (1)$$

Under phase-locked operation, the synchronous reference frame becomes aligned with the grid-voltage vector. Consequently, the quadrature-axis component approaches zero and is selected as the PLL phase-error signal as defined in (2).

$$e(t) = V_q(t) \quad (2)$$

with $V_q(t) \to 0$ under the locked condition.

B. Parallel Dual-MAF Processing

The phase-error signal $e(t)$ is simultaneously processed by two moving-average filters having different window lengths T_1 and T_2 where $T_2 > T_1$. The moving-average operation over a window T is expressed in (3).

$$MAF_T\{x(t)\} = \frac{1}{T}\int_{t-T}^{t} x(\tau)\,d\tau \quad (3)$$

Accordingly, the two MAF-1 and MAF-2 outputs are obtained from (4) and (5), respectively.

$$e_1(t) = \frac{1}{T_1}\int_{t-T_1}^{t} e(\tau)\,d\tau \quad (4)$$

and

$$e_2(t) = \frac{1}{T_2}\int_{t-T_2}^{t} e(\tau)\,d\tau \quad (5)$$

For the nominal grid period $T_g = \frac{1}{f_0}$, the two averaging windows are selected according to (6).

$$T_1 = 0.5T_g, \qquad T_2 = T_g \quad (6)$$

Thus, MAF-1 provides comparatively faster tracking, whereas MAF-2 provides stronger attenuation of oscillatory components. Both MAFs operate on the same q-axis synchronization-error signal.

C. Adaptive Dual-MAF Weighting

The two filtered outputs are combined using the adaptive coefficients $w_1(k)$ and $w_2(k)$ and the resulting PLL error is expressed in (7).

$$e_{PLL}(k) = w_1(k)e_1(k) + w_2(k)e_2(k) \quad (7)$$

The adaptive coefficients satisfy the complementary and bounded-weight constraints given in (8).

$$w_1(k)+w_2(k)=1, \quad 0\le w_1(k), w_2(k)\le 1 \tag{8}$$

Using the complementary relation in (8), the weighted PLL error can be rewritten as shown in (9)

$$e_{PLL}(k)=e_2(k)+w_1(k)\left[e_1(k)-e_2(k)\right] \tag{9}$$

The difference between the two MAF outputs is defined in (10) as the adaptation-driving signal.

$$\Delta e(k)=e_1(k)-e_2(k) \tag{10}$$

Based on this difference, the instantaneous synchronization-error objective function is formulated in (11).

$$J(k)=\frac{1}{2}e_{PLL}^2(k) \tag{11}$$

Differentiating (11) with respect to ω_1 gives the gradient in (12).

$$\frac{\partial J(k)}{\partial w_1}=e_{PLL}(k)\Delta e(k) \tag{12}$$

Using the gradient in (12), the normalized weight-update law is obtained as (13).

$$\tilde{w}_1(k+1)=w_1(k)-\mu(k)\frac{e_{PLL}(k)\Delta e(k)}{\varepsilon+\Delta e^2(k)} \tag{13}$$

Here, $\mu(k)>0$ denotes the adaptation step size and $\varepsilon>0$ is a small regularization constant that prevents numerical ill-conditioning when $\Delta e(k)$ approaches zero.

The unconstrained weight obtained from (13) is projected onto a prescribed interval according to (14).

$$w_1(k+1)=proj_{[w_{\min},w_{\max}]}\left\{\tilde{w}_1(k+1)\right\}, \quad w_2(k+1)=1-w_1(k+1) \tag{14}$$

The projection operator is defined as

$$proj_{[w_{\min},w_{\max}]}(x)=\begin{cases} w_{\min}, & x<w_{\min}, \\ x, & w_{\min}\le x\le w_{\max}, \\ w_{\max}, & x>w_{\max}, \end{cases}$$

This operation prevents unbounded weight variation while preserving the complementary relationship between the two MAF paths. For digital implementation, the two weighted product signals are defined in (15), and their sum yields the PLL error used at the current sampling instant.

$$p_1(k)=w_1(k)e_1(k), \quad p_2(k)=w_2(k)e_2(k) \tag{15}$$

D. Disturbance Index and Adaptive Rate

A bounded synchronization-disturbance index is introduced to regulate the adaptation rate. To avoid introducing additional voltage or THD estimators, the bounded disturbance index is derived directly from the MAF-output disagreement as defined in (16).

$$D(k)=sat_{[0,1]}\left[\frac{|\Delta e(k)|}{E_N+\varepsilon_D}\right] \tag{16}$$

Where $E_N>0$ is a selected normalization level, $\varepsilon_D>0$ prevents numerical singularity, and $sat_{[0,1]}\{.\}$ restricts the index to the interval [0,1].

Using the disturbance index in (16), the adaptive step size is scheduled according to (17).

$$\mu(k)=\mu_{\min}+(\mu_{\max}-\mu_{\min})D(k) \tag{17}$$

Where $0<\mu_{\min}\le\mu_{\max}$. A small value of D(k) therefore produces slower weight adaptation, whereas a larger difference between the two MAF outputs increases the adaptation rate.

E. Adaptive PLL Gain Regulation

The bounded index in (16) is also used to schedule the PLL natural frequency within predefined limits as expressed in (18).

$$\omega_{n,PLL}(k)=\omega_{n,\min}+(\omega_{n,\max}-\omega_{n,\min})D(k) \tag{18}$$

For a damping ratio ζ and small-signal phase-detector gain K_d, the corresponding PLL gains are obtained from (19).

$$K_{p,PLL}(k)=\frac{2\zeta\omega_{n,PLL}(k)}{K_d},\qquad K_{i,PLL}(k)=\frac{\omega_{n,PLL}^2(k)}{K_d} \tag{19}$$

Here, K_d denotes the small-signal gain from phase-angle error to the q-axis phase-detector output around the locked operating point. Its value must correspond to the voltage scaling and Park transformation adopted in the implementation. The adaptively weighted PLL error is processed using the gains in (19). In discrete form, the integral state and angular-frequency correction are evaluated according to (20).

$\xi(k)=\xi(k-1)+T_s e_{PLL}(k)$, and the angular-frequency correction is

$$\Delta\omega(k)=K_{p,PLL}(k)e_{PLL}(k)+K_{i,PLL}(k)\xi(k) \tag{20}$$

F. Frequency and Phase-Angle Estimation

The estimated instantaneous grid angular frequency is obtained by adding the PLL correction to the nominal angular frequency as given in (21).

$$\hat{\omega}(k)=\omega_0+\Delta\omega(k),\qquad \omega_0=2\pi f_0 \tag{21}$$

Finally, the estimated phase angle is calculated from (22) and fed back to synchronous transformation to close the PLL loop.

$$\hat{\theta}(k)=\hat{\theta}(k-1)+T_s\hat{\omega}(k) \tag{22}$$

The calculated angle is fed back to the abc − to − dq transformation, thereby closing the synchronization loop. At the locked condition,

$$V_q(k)\to 0 \quad\Rightarrow\quad \hat{\theta}(k)\to\theta(k)$$

The proposed control structure therefore incorporates two coordinated adaptive mechanisms. The first modifies the relative contribution of the short- and long-window MAF paths through normalized-gradient weighting with projection and complementary constraints. The second schedules the PLL dynamics within bounded limits according to the MAF-output disagreement. Together, these mechanisms provide a structured means of balancing disturbance attenuation and synchronization response while retaining compact control architecture suitable for digital implementation in the DSTATCOM.

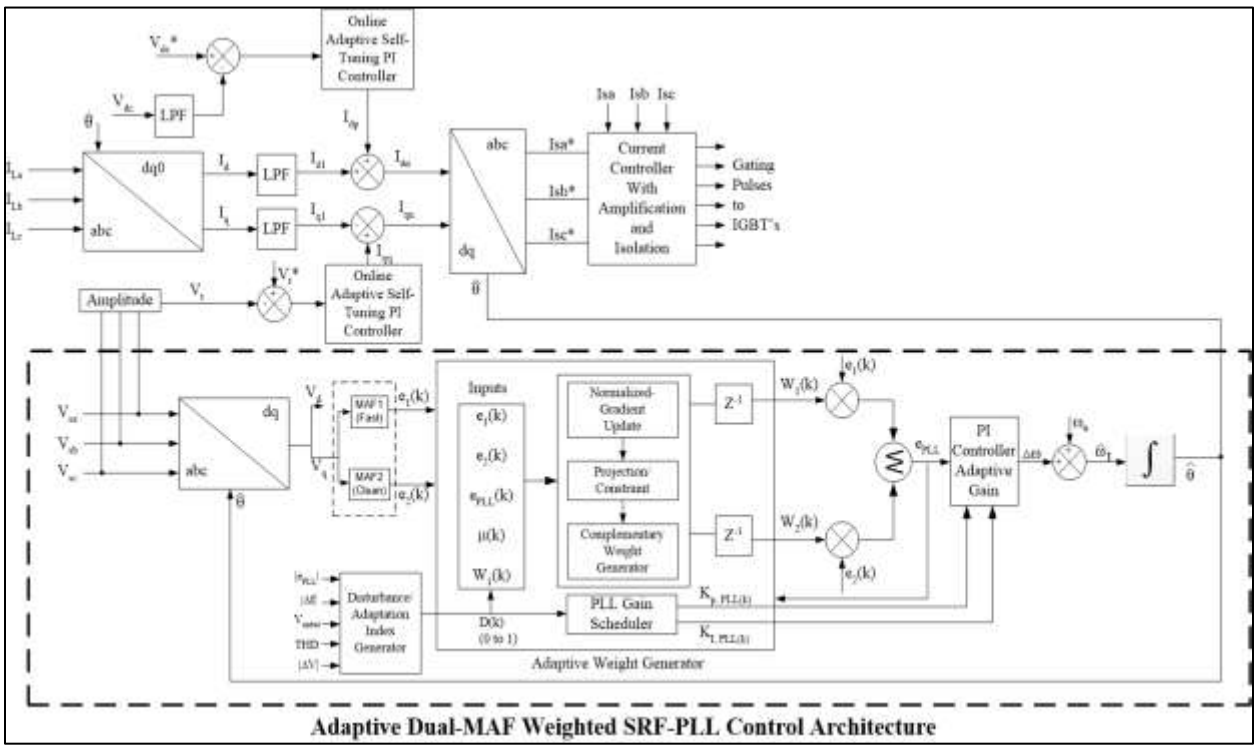


Fig. 2. Adaptive Dual-MAF Weighted SRF-PLL Control with Online Adaptive Self-Tuning PI Regulation for DSTATCOM.

3.1 Online adaptive self-tuning PI control for the DSTATCOM outer loops

The outer control loops of the DSTATCOM regulate the DC-link voltage and the PCC voltage magnitude. In fixed-gain PI control, the proportional and integral gains are selected for a nominal operating condition and remain unchanged during operation. Under sudden load changes, nonlinear loading, or grid-voltage disturbances, such fixed gains may not provide the same transient and steady-state performance over the entire operating range. To improve the dynamic regulation capability, an online adaptive self-tuning PI structure is employed for both the DC-link and PCC-voltage loops. The use of online adaptive PI regulation for STATCOM voltage control has previously been demonstrated by Xu and Li [25], where the controller gains were adjusted dynamically with changes in system operating conditions. Motivated by this adaptive-control principle, a bounded error-dependent self-tuning PI structure is adopted here for the DC-link and PCC-voltage loops of the proposed DSTATCOM The controller preserves the conventional PI form, while Kp and Ki are updated continuously within predefined bounds according to the instantaneous control error.

3.1.1 DC-link voltage control

The DC-link voltage error is defined as in (23), and the corresponding bounded normalized error index is evaluated as using (24).

$$e_{dc}(k) = V_{dc}^{*}(k) - V_{dc}(k) \tag{23}$$

$$\rho_{dc}(k) = \frac{|e_{dc}(k)|}{|e_{dc}(k)| + E_{dc}}, \qquad 0 \le \rho_{dc}(k) < 1 \tag{24}$$

where V_{dc}^{*} is the reference DC-link voltage, V_{dc} is the measured DC-link voltage, and $E_{dc} > 0$ is an error-scaling constant. Since ρ_{dc} remains bounded between zero and unity, it can be used directly as a scheduling variable for the PI gains.

Based on the normalized index in (24), the proportional and integral gains are updated online according to (25) while satisfying the prescribed gain bounds.

$$\begin{aligned} k_{p,dc}(k) &= k_{\rho,dc}^{\min} + \left(k_{\rho,dc}^{\max} - k_{\rho,dc}^{\min}\right)\rho_{dc}(k), \\ k_{i,dc}(k) &= k_{i,dc}^{\min} + \left(k_{i,dc}^{\max} - k_{i,dc}^{\min}\right)\rho_{dc}(k) \end{aligned} \tag{25}$$

subject to

$$k_{\rho,dc}^{\min} \le k_{\rho,dc}(k) \le k_{\rho,dc}^{\max}, \quad k_{i,dc}^{\min} \le k_{i,dc}(k) \le k_{i,dc}^{\max}$$

Accordingly, a larger DC-link voltage error shifts the controller gains toward their upper bounds, whereas the gains move toward the lower bounds as the voltage approaches its reference. This provides stronger corrective action during large deviations and smoother operation near steady state.

Let $x_{dc}(k)$ denote the integral state of the DC-link PI controller. Using the adaptive gains obtained from (25), the unconstrained active-current command is generated and subsequently limited as expressed in (26).

$$\begin{aligned} I_{dp}^{u}(k) &= K_{p,dc}(k)e_{dc}(k) + x_{dc}(k) \\ I_{dp}^{u}(k) &= sat\left[I_{dp}^{u}(k), I_{dp}^{\min}, I_{dp}^{\max}\right] \end{aligned} \tag{26}$$

The saturation operator can be written as

$$sat(x, x_{\min}, x_{\max}) = \min\left[x_{\max}, \max(x_{\min}, x)\right]$$

To prevent integral windup during current saturation, the integral state is updated through back-calculation mechanism given in (27).

$$x_{dc}(k+1) = x_{dc}(k) + T_s\left[K_{i,dc}(k)e_{dc}(k) + k_{aw,dc}\left(I_{dp}(k) - I_{dp}^{u}(k)\right)\right] \tag{27}$$

where T_s denotes the sampling period and $K_{aw,dc}$ is the anti-windup gain. When no saturation occurs, $I_{dp} = I_{dp}^{u}$, so the anti-windup term becomes zero. The resulting active-current component is combined with the fundamental d-axis load-current component according to (28) to obtain the commanded d-axis source-current component.

$$I_{dn}(k) = I_{d1}(k) + I_{dp}(k) \tag{28}$$

3.1.2 PCC-voltage control

For the PCC-voltage loop, the instantaneous voltage error is defined in (29) and its bounded normalized adaptation index is obtained from (30).

$$e_{t}(k) = V_{t}^{*}(k) - V_{t}(k) \tag{29}$$

and

$$\rho_t(k)=\frac{|e_t(k)|}{|e_t(k)|+E_t},\qquad 0\le\rho_t(k)<1 \tag{30}$$

where V_t^* is the PCC-voltage reference, V_t is the measured PCC-voltage magnitude, and $E_t>0$ is the corresponding error-scaling constant. The online proportional and integral gains are subsequently scheduled according to (31) within their prescribed limits.

$$\begin{aligned}k_{p,t}(k)&=k_{\rho,t}^{\min}+\left(k_{\rho,t}^{\max}-k_{\rho,t}^{\min}\right)\rho_t(k),\\ k_{i,t}(k)&=k_{i,t}^{\min}+\left(k_{i,t}^{\max}-k_{i,t}^{\min}\right)\rho_t(k)\end{aligned} \tag{31}$$

with

$$k_{\rho,t}^{\min}\le k_{\rho,t}(k)\le k_{\rho,t}^{\max},\quad k_{i,t}^{\min}\le k_{i,t}(k)\le k_{i,t}^{\max}$$

Using the adaptive gains in (31), the reactive-current command is generated and constrained as expressed as in (32).

$$I_{qq}^{u}(k)=K_{p,t}(k)e_t(k)+x_t(k)$$

and the current-limited output is

$$I_{qq}(k)=sat\left[I_{qq}^{u}(k),I_{qq}^{\min},I_{qq}^{\max}\right] \tag{32}$$

The corresponding integral state is updated using the back-calculation anti-windup relation given in (33).

$$x_t(k+1)=x_t(k)+T_s\left[K_{i,t}(k)e_t(k)+k_{aw,t}\left(I_{qq}(k)-I_{qq}^{u}(k)\right)\right] \tag{33}$$

The resulting q-axis reference-current component is obtained from (34).

$$I_{qn}(k)=I_{qq}(k)-I_{q1}(k) \tag{34}$$

The d-and q-axis reference-current components obtained from (28) and (34) are transformed into the three-phase reference currents according to (35) using the phase angle $\hat{\theta}(k)$ estimated by the Adaptive Dual-MAF Weighted SRF-PLL:

$$\begin{bmatrix}i_{sa}^{*}(k)\\ i_{sb}^{*}(k)\\ i_{sc}^{*}(k)\end{bmatrix}=T_{dq\to abc}\left(\hat{\theta}(k)\right)\begin{bmatrix}I_{dn}(k)\\ I_{qn}(k)\end{bmatrix} \tag{35}$$

Thus, the adaptive self-tuning PI mechanism modifies only the generation of the active and reactive current-control components I_{dp} and I_{qq}. Three-phase references (I_{sa}^{*}, I_{sb}^{*}, I_{sc}^{*}) set currents for harmonic suppression, load balancing, and reactive compensation. Comparison with sensed currents generates errors for a hysteresis controller, which outputs inverter gating pulses for fast tracking and near-sinusoidal currents.

Table 1. Hardware parameters of the experimental DSTATCOM

System quantities	Values
Supply voltage	3Ø, 120 V (L–L), 50 Hz
PCC ripple filter	R_f =5Ω, C_f =10 μF
Interfacing inductor	L_f =2.5 mH
Non linear load	A three-phase uncontrolled rectifier feeding an R–L load (15 Ω, 60 mH).
VSI parameters	DC capacitor (C_{dc}): 1650 μF; reference DC link voltage (Vdc): 220 V;
Hysteresis band(h)	± 0.5A

4. Experimental validation and discussion

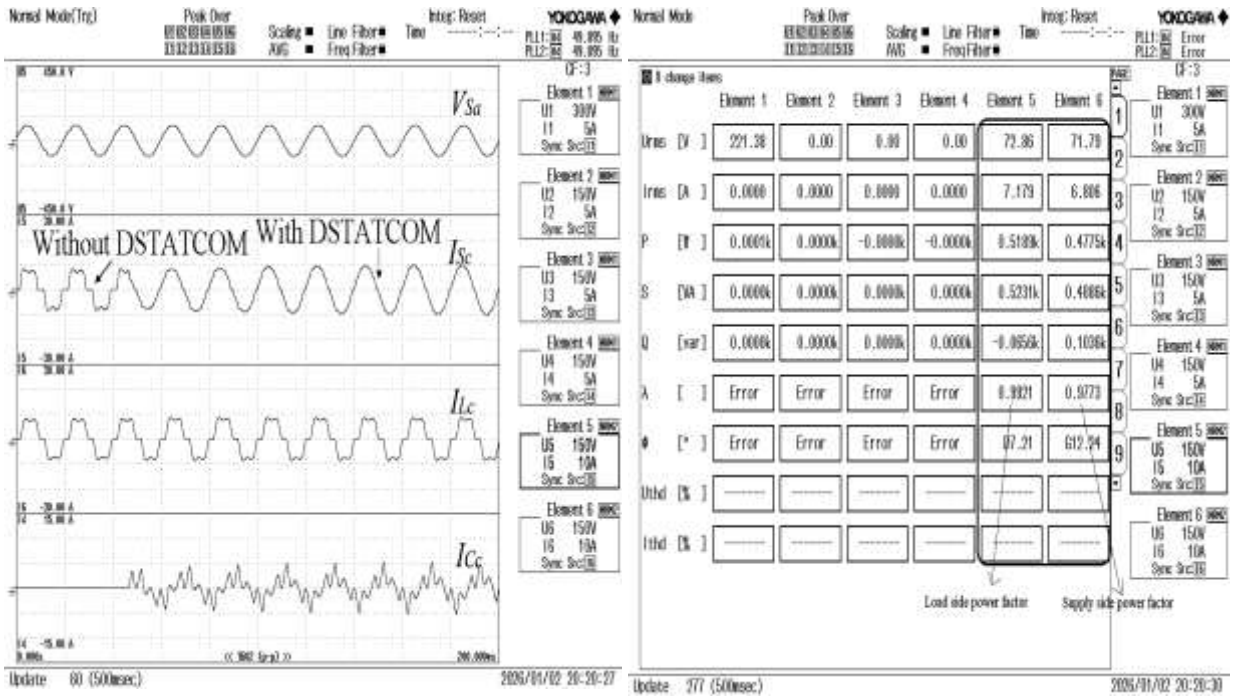
The experimental performance of the proposed Adaptive Dual-MAF Weighted SRF-PLL-controlled DSTATCOM is investigated under steady-state, unbalanced, and dynamic nonlinear-load conditions as shown in Fig.3. The prototype is operated from a three-phase, 120-V (line-to-line), 50-Hz supply and employs a 1650 μF DC-link

capacitor, with the reference voltage maintained at 220 V. A three-phase uncontrolled rectifier feeding a 15 Ω and 60 mH R –L load is considered as the nonlinear load. The DSTATCOM is interfaced through 2.5 mH coupling inductors, and a hysteresis band of ±0.5 A is employed for current tracking. The experimental investigation evaluates harmonic suppression, reactive-power compensation, source-current balancing, DC-link voltage regulation, and transient recovery during load variations. The principal system and control parameters used for the experimental study are listed in Table 1.

Fig. 3. Experimental prototype of the FPGA-based DSTATCOM.

4.1 Steady-State Compensation Performance Under Nonlinear Loading

Fig. 4(a) depicts the measured steady-state response before and after activation of the DSTATCOM. Before compensation, the source current follows the distorted current demanded by the nonlinear load. After the DSTATCOM is connected, the injected compensating current supplies the dominant harmonic and reactive components, causing the source current to become nearly sinusoidal and closely aligned with the PCC voltage. Fig. 4(b) presents the corresponding numerical measurements obtained from the power-quality analyzer, providing quantitative confirmation of the source- and load-side electrical quantities. The observed source-side power-factor improvement toward unity demonstrates effective reactive-power compensation under nonlinear loading.



(a) **(b)**

Fig.4. Experimental steady-state performance under nonlinear loading: (a) source, load, and compensating current waveforms before and after DSTATCOM compensation; (b) measured source- and load-side electrical quantities.

The harmonic compensation capability is further examined in Fig. 5. Figs. 5(a)–(c) depict the PCC line voltage Vab together with the phase-a, phase-b, and phase-c source currents I_{Sa}, I_{Sb}, and I_{Sc}, respectively, and their corresponding harmonic spectra. The compensated source currents retain nearly sinusoidal waveforms despite the nonlinear current demanded by the rectifier load. Fig. 5(d) provides the numerical analyzer results. The measured rms source currents are 6.98 A, 6.93 A, and 7.00 A, while the corresponding THDs are 3.52%, 3.49%, and 3.91% for phases a, b, and c, respectively.

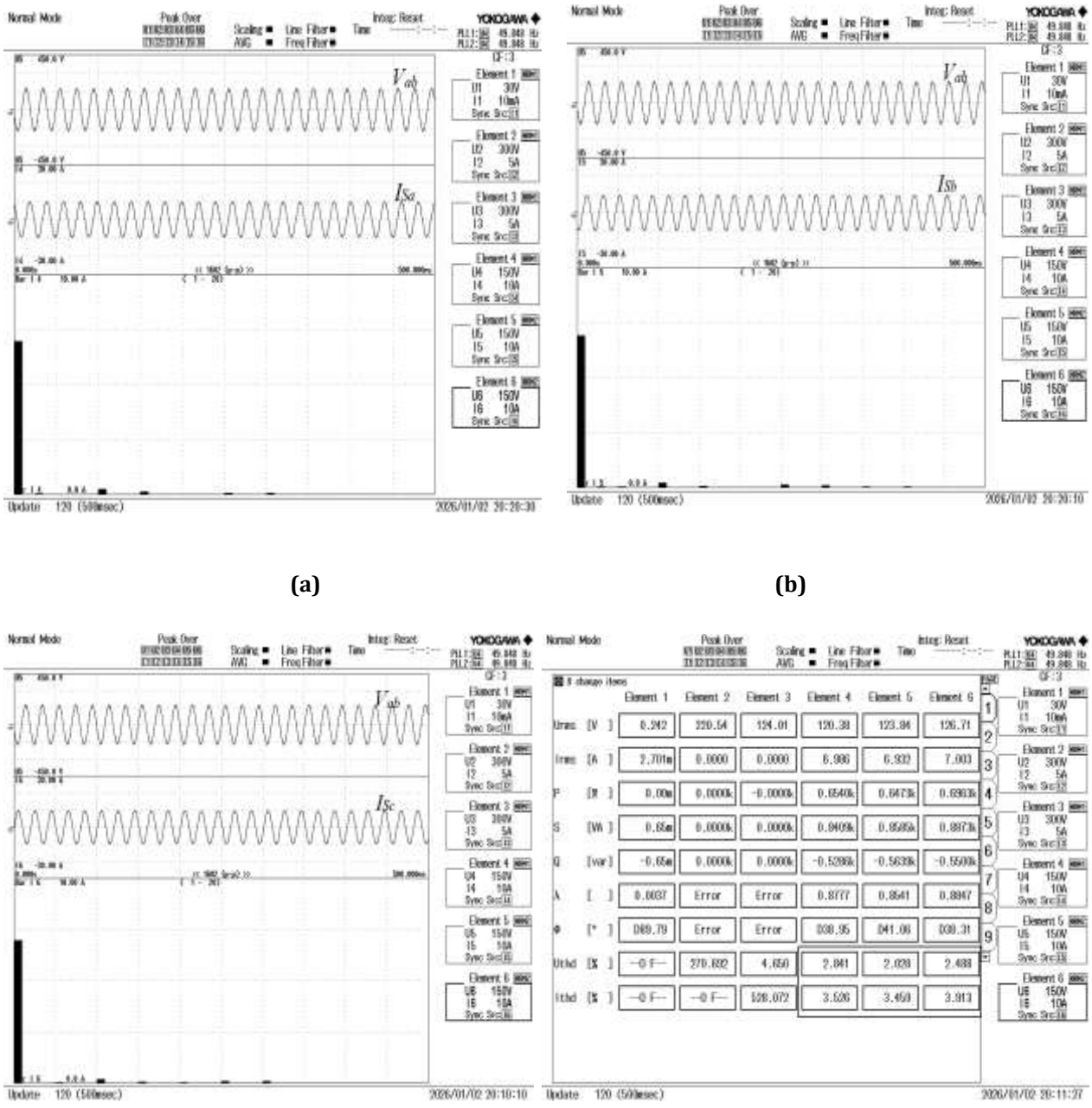


Fig. 5. Experimental harmonic performance under nonlinear loading: (a) V_{ab}, I_{Sa} and harmonic spectrum of I_{Sa}; (b) V_{ab}, I_{Sb} and harmonic spectrum of I_{Sb}; (c) V_{ab}, $I_{SC}$and harmonic spectrum of I_{SC}; (d) measured RMS values and THD of the three-phase source currents.

The average source-current THD is approximately 3.64%, while the close agreement among the three RMS current values confirms satisfactory current balancing. The results demonstrate that the proposed synchronization and compensation scheme enables the DSTATCOM to isolate a substantial portion of the nonlinear-load harmonic demand from the source. The simultaneous improvement in current waveform

quality and power factor confirms effective harmonic and reactive-current compensation during steady-state operation.

4.2 Load Balancing Performance of DSTATCOM under Nonlinear Load

The load-balancing capability of the proposed control scheme is evaluated in Fig. 6 by introducing a phase-c load transition. Fig. 6(a) depicts the three-phase nonlinear load currentsI_{La},I_{Lb}, and I_{Lc}, where the phase-c switching event produces an intentionally unbalanced load condition. Figs. 6(b)–(d) show the corresponding phase source currentsI_{Sa},I_{Sb} and I_{SC} respectively, together withV_{ab}.

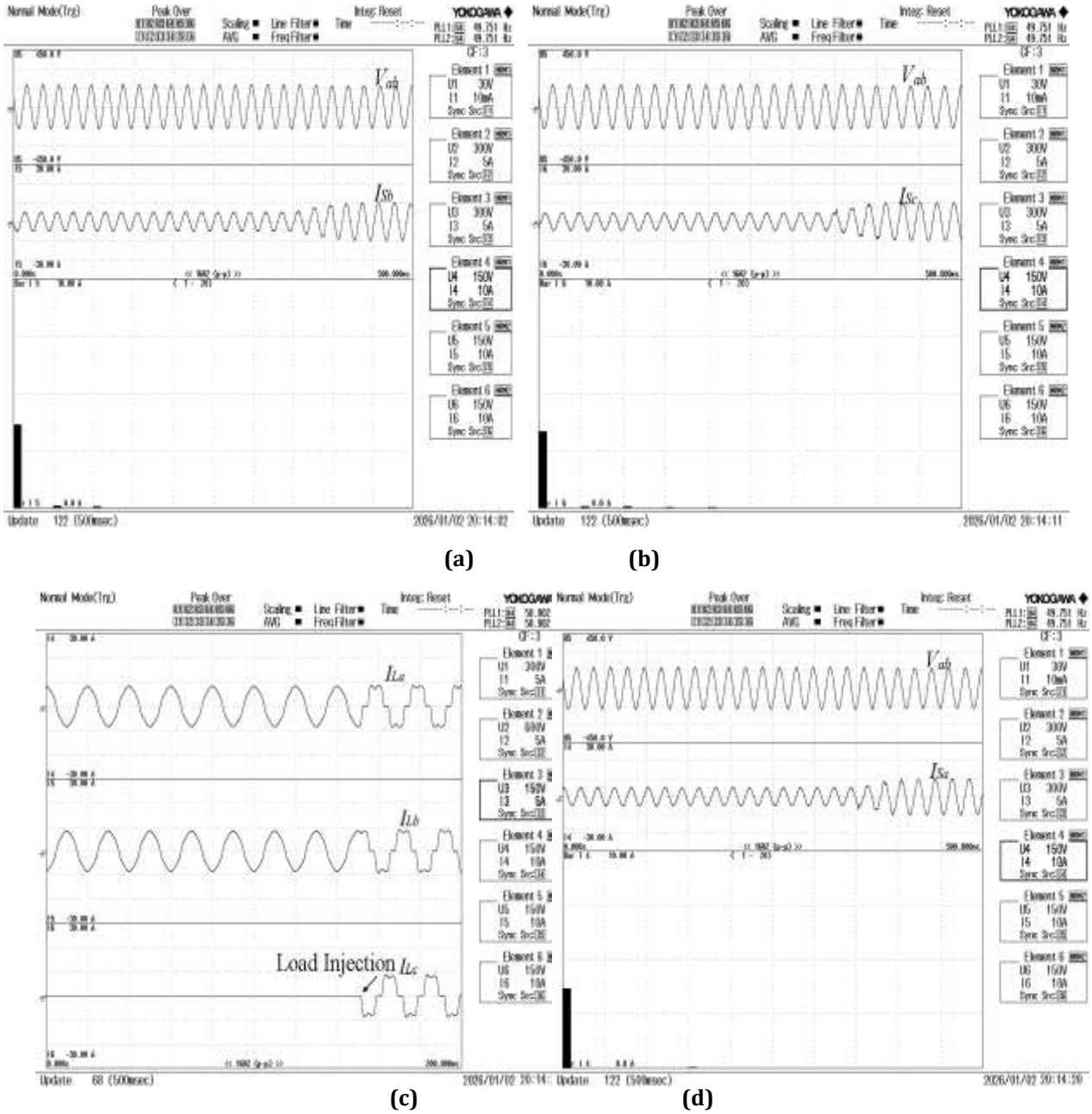


Fig.6. Experimental load-balancing performance under nonlinear loading: (a) three-phase load currentsI_{Sa}, I_{Sb} and I_{SC} during phase-c load switching; (b) V_{ab} and I_{Sa}; (c) $V_{ab}$and I_{Sb}; (d) V_{ab} and I_{SC}.

Although the phase-c load current undergoes a pronounced change, the corresponding source currents remain substantially balanced because the DSTATCOM modifies the compensating-current demand according to the changed load condition. The disturbance component associated with the load imbalance is therefore largely supplied by the compensator rather than transferred to the upstream source. The maintained sinusoidal nature ofI_{Sa},I_{Sb}, and I_{SC} also indicates that synchronization is preserved during the phase-c transition. These results

establish the ability of the proposed controller to perform load balancing concurrently with harmonic-current compensation under unbalanced nonlinear loading.

4.3 Dynamic Response of DSTATCOM under Nonlinear Load

The dynamic performance of the proposed controller during phase-cc nonlinear-load switching is presented in Fig. 7. Fig. 7(a) depicts V_{ab} and the three-phase source currentsI_{Sa},I_{Sb}, and I_{SC}. Despite the abrupt phase-c load transition, the source currents exhibit only a short transient disturbance and subsequently recover their balanced operating condition. Fig. 7(b) shows V_{ab} together with the nonlinear load currents I_{La},I_{Lb}, and I_{Lc} the abrupt variation of I_{Lc} clearly identifies the imposed phase-c load switching event. Fig. 7(c) presents V_{ab} and the compensating currentsI_{Ca}, I_{Cb} and I_{CC}. The change in I_{CC} following the disturbance demonstrates the redistribution of compensating current required to maintain the desired source-current condition.

Fig. 7(d) provides a more focused assessment of the transient by simultaneously displaying V_{dc},I_{SC}, I_{LC}, and I_{CC}. The phase-c load current changes abruptly at the switching instant, while the compensating current responds correspondingly to accommodate the new load demand. Consequently, the disturbance transferred to I_{SC} is limited and the source current returns rapidly toward its compensated steady-state condition. The DC-link voltage remains nearly constant during the load transition, demonstrating that the DC-side energy balance is maintained despite the sudden change in compensating-current demand.

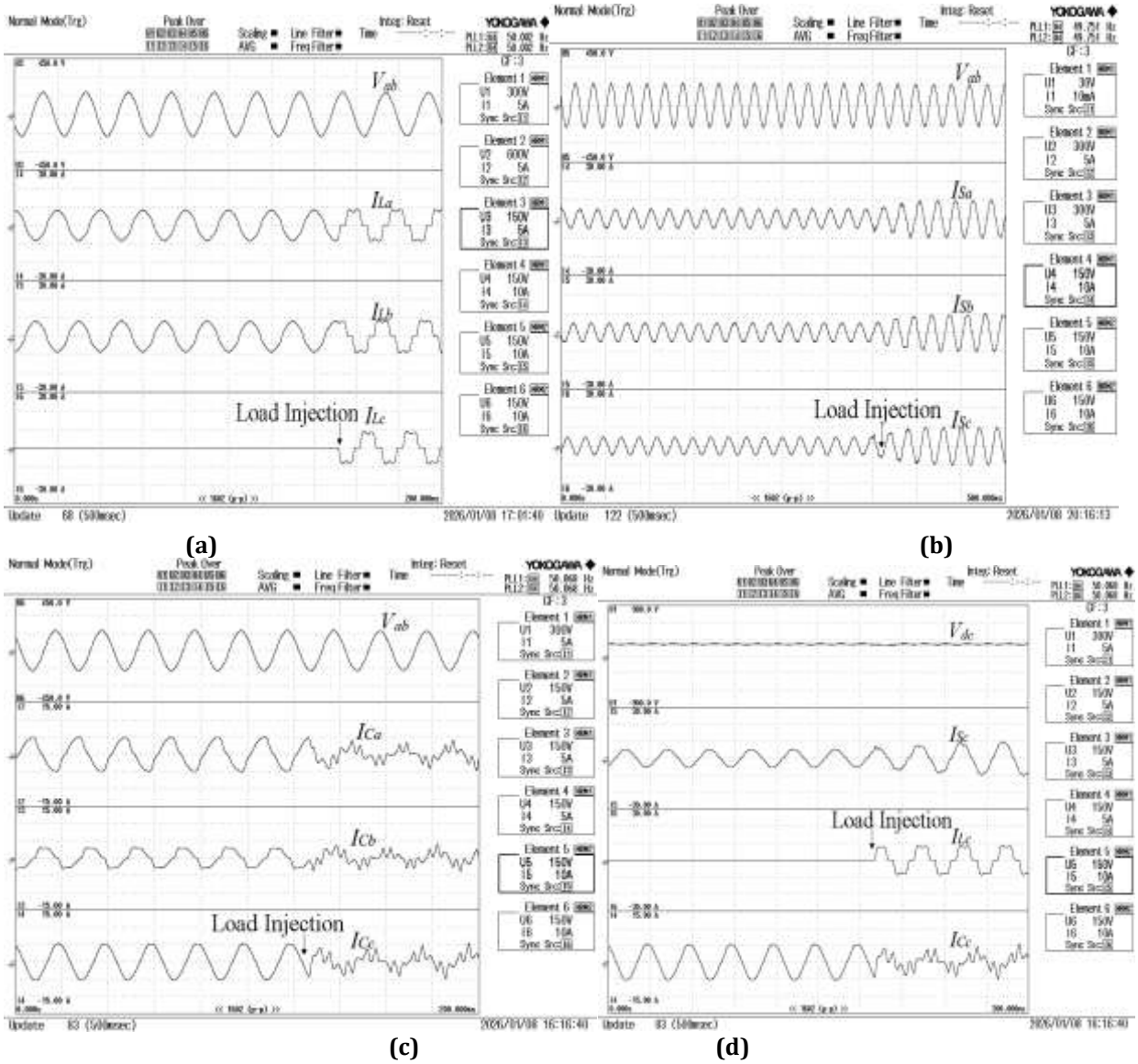


Fig.7. Experimental dynamic response during phase-cc nonlinear-load switching: (a) V_{ab} with source currents I_{Sa}, $I_{Sb}$and I_{SC}; (b) $V_{ab}$with load currents I_{La},I_{Lb}, and I_{Lc}; (c) V_{ab} with compensating currents I_{Ca}, I_{Cb} and I_{CC}; (d) DC-link voltage V_{dc} source current I_{SC} , load current I_{LC}, and compensating current I_{CC} during the load transition.

For the 50-Hz system, one fundamental cycle corresponds to 20 ms. The measured waveforms show that the principal current disturbance is confined to the immediate switching interval without sustained oscillation. More importantly, the phase-c load transition does not produce loss of synchronization or prolonged DC-link voltage deviation. The coordinated response of I_{LC}, I_{CC}, I_{SC}, and V_{dc} demonstrates that the Adaptive Dual-MAF Weighted SRF-PLL, reference-current generation, outer voltage regulation, and current controller remain stable during the nonlinear-load transient. Collectively, the experimental results demonstrate the effectiveness of the proposed controller over three distinct operating conditions. Under steady-state nonlinear loading, source-current THDs of 3.52%, 3.49%, and 3.91% are obtained for phases a, b, and c, respectively. Under unbalanced loading, the source currents remain substantially balanced despite the phase-c load variation. During dynamic operation, the compensating current responds to the abrupt change in load demand while the DC-link voltage remains regulated. The results therefore verify simultaneous harmonic mitigation, reactive-power compensation, load balancing, and stable transient operation of the proposed DSTATCOM control scheme.

5. Conclusion

This paper presented an Adaptive Dual-MAF Weighted SRF-PLL with online self-tuning PI regulation for a three-phase VSC-based DSTATCOM operating under nonlinear, unbalanced, and dynamically varying load conditions. The synchronization scheme employs parallel short- and long-window MAF paths to retain complementary tracking and filtering characteristics. Their contributions are adjusted online through a normalized-gradient update, while projection and complementary-weight constraints maintain bounded adaptive coefficients. A disturbance-dependent adaptation mechanism further modifies the weight-update rate and PLL dynamics according to the instantaneous difference between the two MAF responses.

The proposed PLL is coordinated with online adaptive self-tuning PI regulators for the DC-link and PCC-voltage outer loops, allowing the controller gains to vary within prescribed limits during changes in operating conditions. FPGA-based experimental validation demonstrates effective harmonic compensation and source-current balancing. The measured source currents are 6.98 A, 6.93 A, and 7.00 A, with corresponding THDs of 3.52%, 3.49%, and 3.91%, giving an average source-current THD of approximately 3.64%. During phase-cc load switching, the source currents remain substantially balanced while the compensating current adjusts to the changed load demand. The DC-link voltage remains regulated around its 220-V reference during the nonlinear-load transition, indicating stable DC-side energy regulation and coordinated transient operation.

Overall, the experimental results demonstrate that the proposed control architecture provides simultaneous harmonic-current mitigation, reactive-power compensation, load balancing, and stable dynamic operation while retaining a control structure suitable for FPGA-based real-time implementation. The adaptive weighting of the Dual-MAF paths and online adjustment of the control parameters provide a systematic extension beyond fixed-filter and fixed-gain DSTATCOM control structures.

References

[1] M. Mishra, Power Quality in Power Distribution Systems: Concepts and Applications, CRC Press, Boca Raton, FL, USA, 2023.

[2] IEC 61000-3-2, Electromagnetic Compatibility – Limits for Harmonic Current Emissions, IEC, 2018.

[3] S. R. Arya, M. M. Patel, S. J. Alam, J. Srikakolapu, and A. K. Giri, "Phase-locked-loop-based algorithms for DSTATCOM to mitigate load-created power quality problems," International Transactions on Electrical Energy Systems, Vol. 30, No. 1, Art. No. e12161, 2020, doi: 10.1002/2050-7038.12161.

[4] S. R. Arya et al., "Compensation of power quality problems through DSTATCOM using various phase locked loops," Electrical Engineering, vol. 104, pp. 45–66, 2022, doi: 10.1007/s00202-021-01341-2.

[5] J. Sharma, C. K. Sundarabalan, C. Balasundar, N. S. Srinath, and J. M. Guerrero, "Unified variable regularization factor based static compensator for power quality enhancement in distribution grid," Electric Power Systems Research, vol. 221, Art. no. 109483, 2023, doi: 10.1016/j.epsr.2023.109483.

[6] P. Bansal and A. Singh, "Control of DSTATCOM with parallel tangent method based adaptive control algorithm under distorted grid conditions," Electric Power Components and Systems, vol. 53, no. 5, pp. 655–667, 2025, doi: 10.1080/15325008.2024.2314208.

[7] A. Ram, P. R. Sharma, and R. K. Ahuja, "Enhancement of power quality using U-SOGI based control algorithm for DSTATCOM," Ain Shams Engineering Journal, vol. 15, no. 1, Art. no. 102296, 2024, doi: 10.1016/j.asej.2023.102296.

[8] B. Mohan, S. Siddhan, and N. Chinnadurai, "Control for power quality improvement of solar photovoltaic-distributed static synchronous compensator interfaced with weak grid using multi-variable filter

dual second-order generalized integrator phase-locked loop," Electric Power Components and Systems, vol. 52, no. 9, pp. 1616–1635, 2024, doi: 10.1080/15325008.2023.2243932.
[9] A. S. Özer, F. Sevilmiş, H. Karaca, and H. Ahmed, "Power quality improvement of DSTATCOM using fast hybrid-PLL-based control method for wind energy applications," Protection and Control of Modern Power Systems, vol. 11, no. 2, pp. 16–34, 2026, doi: 10.23919/PCMP.2025.000070.
[10] A. S. Özer, F. Sevilmiş, and H. Karaca, "A moving average filter based DSTATCOM control approach," Electrical Engineering and Energy, vol. 4, no. 1, pp. 1–10, 2025, doi: 10.64470/elene.2025.1001.
[11] G. Escobar, L. Ibarra, J. E. Valdez-Resendiz, J. C. Mayo-Maldonado, and D. Guillen, "Nonlinear stability analysis of the conventional SRF-PLL and enhanced SRF-EPLL," IEEE Access, vol. 9, pp. 59446–59455, 2021, doi: 10.1109/ACCESS.2021.3073063.
[12] C. Liu, J. Jiang, J. Jiang, and Z. Zhou, "Enhanced grid-connected phase-locked loop based on a moving average filter," IEEE Access, vol. 8, pp. 5308–5315, 2020, doi: 10.1109/ACCESS.2019.2963362.
[13] F. O. Martinz, R. Destro, N. R. N. Ama, K. C. M. de Carvalho, W. Komatsu, and L. M. Junior, "Modeling and design of a fast-dynamic response phase-locked loop based on moving average filter," Eletrônica de Potência, vol. 25, no. 1, pp. 114–124, 2019.
[14] J. Li, Q. Wang, L. Xiao, Y. Hu, Q. Wu, and Z. Liu, "An α-β-frame moving average filter to improve the dynamic performance of phase-locked loop," IEEE Access, vol. 8, pp. 180661–180671, 2020,
doi: 10.1109/ACCESS.2020.3028237.
[15] W. Luo and D. Wei, "A frequency-adaptive improved moving-average-filter-based quasi-type-1 PLL for adverse grid conditions," IEEE Access, vol. 8, pp. 54145–54153, 2020,
doi: 10.1109/ACCESS.2020.2981426.
[16] Z. Wang, P. Fu, L. Huang, X. Chen, S. He, X. Zhang, and J. Yang, "Performance improvement of a three-phase PLL under distorted grid conditions based on frequency adaptive hybrid pre-filtering," IET Power Electronics, vol. 15, pp. 1429–1440, 2022, doi: 10.1049/pel2.12314.
[17] P. Taheri, J. Amini, and M. Moallem, "Improving performance of three-phase MAF-PLL under asymmetrical DC-offset condition," IEEE Access, vol. 11, pp. 111200–111211, 2023,
doi: 10.1109/ACCESS.2023.3322430.
[18] P. Taheri, J. Amini, and M. Moallem, "Variable window size moving average filter for phase-locked-loop synchronization," IEEE Access, vol. 12, pp. 88111–88121, 2024,
doi: 10.1109/ACCESS.2024.3417179.
[19] I. A. Smadi, H. A. Kreashan, and I. E. Atawi, "Enhancing the filtering capability and the dynamic performance of a third-order phase-locked loop under distorted grid conditions," Energies, vol. 16, no. 3, Art. no. 1472, 2023, doi: 10.3390/en16031472.
[20] A. C. Kathiresan, J. PandiaRajan, A. Sivaprakash, T. Sudhakar Babu, and M. R. Islam, "An adaptive feed-forward phase locked loop for grid synchronization of renewable energy systems under wide frequency deviations," Sustainability, vol. 12, no. 17, Art. no. 7048, 2020, doi: 10.3390/su12177048.
[21] A. Kumar, A. Deb, J. G. Sreenath, P. Tripathy, and R. Adda, "A robust grid synchronization technique using a novel comb filter-based PLL under distorted grid conditions," Electric Power Systems Research, vol. 257, Art. no. 112959, 2026, doi: 10.1016/j.epsr.2026.112959.
[22] R. Jayaraman and A. A. Victoire, "Implementation of differential equation of single-phase source-load system based control algorithm for three-phase DSTATCOM under stiff source," Electric Power Components and Systems, vol. 45, no. 18, pp. 1985–1995, 2017,
doi: 10.1080/15325008.2017.1362606.
[23] R. Jayaraman, S. Thamizharasan, J. Baskaran, V. Meena, J. Bahadur, and V. K. Jadoun, "High-efficiency multilevel inverter topology with minimal switching devices for enhanced power quality and reduced losses," IET Power Electronics, vol. 18, no. 1, Art. no. e12851, 2025, doi: 10.1049/pel2.12851.
[24] L. J. Varghese, R. Jayaraman, K. Cherukupalli, and H. Senthamarai, "Performance analysis of microgrid using wind power based on steady-state voltage stability," Electric Power Components and Systems, Vol. 51, No. 20, pp. 2464–2473, 2023, doi: 10.1080/15325008.2023.2210567.
[25] Y. Xu and F. Li, "Adaptive PI Control of STATCOM for Voltage Regulation," IEEE Transactions on Power Delivery, vol. 29, no. 3, pp. 1002–1011, June 2014, doi: 10.1109/TPWRD.2013.2291576.